EXHIBIT A

PARTIES' AMENDED JOINT CLAIM CONSTRUCTION CHART

FOR FAMILY 3 PATENTS

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"transceiver"	'890 patent, claim 5 '381 patent, claim 5 '882 patent, claim 13 '048 patent, claim 1 '473 patent, claim 19, 28 '126 patent, claims 1, 10	"communications device capable of transmitting and receiving data wherein the transmitter portion and receiver portion share at least some common circuitry" Intrinsic Evidence: Ex. B ('890 patent), Fig. 1, 3:61-62, 5:4-17, and 6:60-64.[1]	"communications device capable of transmitting and receiving data"
"shared memory"	'890 patent, claim 5 '381 patent, claim 5 '882 patent, claim 13 '048 patent, claim 1	"a common memory space used by at least two functions, where particular memory cells within the common memory space can be used by either one of the functions" Intrinsic Evidence: Ex. B ('890 patent), Fig. 1 (Shared Memory 120), 4:5-13, 4:23-28, 5:10-17, 5:33-57, 5:65 – 6:3, and 9:28-37	"single common memory in a transceiver used by at least two functions corresponding to at least two latency paths"
"amount of memory"	'890 patent claim 5 ' 381 patent, claim 5 '882 patent, claim 13 '048 patent, claim 1	plain meaning or "number of units of memory" Intrinsic Evidence: Ex. B ('890 patent), Fig. 3 (S310 and S320), 1:65 – 2:3, 6:29-33, and 6:42-46	"number of bytes of memory"

[1] The '890, '381, '882, '048, '473, and '126 share a common disclosure. For brevity, this document cites only to the '890 patent.

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
"wherein at least a portion of the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the message"	'473 patent, claim 19 '126 patent, claim 1	"at least some particular memory cells within the memory can be allocated for use by either the [first] interleaving function or [second interleaving / deinterleaving] function at any one particular time depending on the message" Intrinsic Evidence: Ex. B ('890 patent), Fig. 3 (S320), Fig. 4 (S420 and S470), 4:5-13, 4:23-40, 5:10-17, 5:33-57, 5:65-6:3, 6:65 – 7:11, 8:9-51, 8:65-9:17, and 9:28-37	"wherein at least a number of bytes within the memory may be allocated to the [first] interleaving function or the [second interleaving / deinterleaving] function at any one particular time depending on the amounts of memory specified in the message"
"portion of the memory"	'473 patent, claims 19, 28 '126 patent, claims 1, 10	This term should not be construed out of context. See above for proposed construction in context.	"number of bytes within the memory"
"memory is allocated between the [first] interleaving function and the [second interleaving/ deinterleaving] function"	'473- claim 19 '126 – claim 1	"an amount of the memory is allocated to the [first] interleaving function and an amount of memory is allocated to the [second interleaving / deinterleaving] function"	"a number of bytes of memory are allocated to the [first] interleaving function and a number of bytes of memory allocated to the [second interleaving/ deinterleaving] function"
"wherein the generated message indicates how the memory has been allocated between the [first deinterleaving / interleaving] function and the [second]	'473 patent, claim 28 '126 patent, claim 10	"wherein the generated message indicates the amount of memory that has been allocated to the [first deinterleaving / interleaving] function and the amount of memory allocated to the [second] deinterleaving function"	"wherein the generated message indicates a number of bytes of memory allocated to the [first deinterleaving / interleaving] function and a number of bytes of memory allocated to the [second] deinterleaving function"

Disputed Claim Term	**Patent, Asserted Claims**	**Plaintiff's Proposed Construction**	**Defendants' Proposed Construction**
deinterleaving function"		Intrinsic Evidence: Ex. B ('890 patent), Fig. 3 (S320), Fig. 4 (S420 and S470), 4:5-13, 4:23-40, 5:10-17, 5:33-57, 5:65-6:3, 6:65-7:11, 8:9-51, 8:65-9:17, and 9:28-37	
"system that allocates shared memory"	'882- claim 13	Not indefinite. *See, e.g., Microprocessor Enhancement Corp. v. Texas Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008)	Indefinite under *IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377 (Fed. Cir. 2005) when viewed in conjunction with the claim elements "a transceiver that performs," "determining an amount of memory . . .," "allocating a first [second] number of bytes," and "deinterleaving the first plurality of RS coded data bytes . . ."
"a multicarrier communications transceiver that is configured to perform"	'473 – claim 19 '126 – claim 1	Not indefinite. *See, e.g., Microprocessor Enhancement Corp. v. Texas Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008)	Indefinite under *IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377 (Fed. Cir. 2005) when viewed in conjunction with the claim elements "wherein the memory is allocated between the [first] interleaving function and the [second interleaving]/ deinterleaving function . . ."
"a multicarrier communications transceiver that is configured to generate"	'126 – claim 10	Not indefinite. *See, e.g., Microprocessor Enhancement Corp. v. Texas Instruments Inc.*, 520 F.3d 1367, 1375 (Fed. Cir. 2008)	Indefinite under *IPXL Holdings, Inc. v. Amazon.com Inc.*, 430 F.3d 1377 (Fed. Cir. 2005) when viewed in conjunction with the

Disputed Claim Term	Patent, Asserted Claims	Plaintiff's Proposed Construction	Defendants' Proposed Construction
			claim elements "wherein the generated message indicates how the memory has been allocated between the first deinterleaving function and the second deinterleaving function . . ."

Claim Term	Patent, Claims	Agreed Construction
"multicarrier"	'473 patent, claim 19, 28 '126 patent, claims 1, 10	"having multiple carrier signals that are combined to produce a transmission signal"
"the shared memory allocated to the [deinterleaver/interleaver] is used at the same time as the shared memory allocated to the [interleaver/deinterleaver]"	'890 patent, claim 5 '381 patent, claim 5 '882 patent, claim 13 '048 patent, claim 1	"the deinterleaver reads from, writes to, or holds information for deinterleaving in its respective allocation of the shared memory at the same time as the interleaver reads from, writes to, or holds information for interleaving in its respective allocation of the shared memory"
"latency path"	'473 patent, claims 19, 28 '126 patent, claims 1, 10	"a transmit or receive path, wherein each path has a distinct, but not necessarily different, latency or delay"